AFRL-RV-PS-
TR-2010-1039

AFRL-RV-PS-
TR-2010-1039

MAGNETIC RANDOM ACCESS MEMORY; INTEGRATED PASSIVE COMPONENTS

Gregory W. Donohoe

University of Idaho
Electrical and Computer Engineering
BEL 210, POB 441023
Moscow, ID 83844-1023

2 June 2010

Final Report

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION IS UNLIMITED

AIR FORCE RESEARCH LABORATORY
Space Vehicles Directorate
3550 Aberdeen Ave SE
AIR FORCE MATERIEL COMMAND
KIRTLAND AIR FORCE BASE, NM 87117-5776

DTIC COPY

NOTICE AND SIGNATURE PAGE

AFRL-RV-PS-TR-2010-1039 HAS BEEN REVIEWED AND IS APPROVED FOR PUBLICATION IN ACCORDANCE WITH ASSIGNED DISTRIBUTION STATEMENT.

//SIGNED//	//SIGNED//
SHANE FRANCIS	WILLIAM A. SCHUM, Lt Col, USAF
Program Manager	Deputy Chief, Spacecraft Technology Division
	Space Vehicles Directorate

REPORT DOCUMENTATION PAGE			*Form Approved* *OMB No. 0704-0188*
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing this collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number. **PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.**			
1. REPORT DATE *(DD-MM-YYYY)* 02-06-2010	**2. REPORT TYPE** Final Report		**3. DATES COVERED** *(From - To)* 01-09-2006 to 30-04-2010
4. TITLE AND SUBTITLE Magnetic Random Access Memory; Integrated Passive Components			**5a. CONTRACT NUMBER** FA9453-06-1-0355
			5b. GRANT NUMBER
			5c. PROGRAM ELEMENT NUMBER 63401F
6. AUTHOR(S) Gregory W. Donohoe			**5d. PROJECT NUMBER** 5159
			5e. TASK NUMBER
			5f. WORK UNIT NUMBER 299060
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) University of Idaho Electrical and Computer Engineering BEL 210, POB 441023 Moscow, ID 83844-1023			**8. PERFORMING ORGANIZATION REPORT NUMBER** MRAM-III INTPASS-I Final
9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES) Air Force Research Laboratory Space Vehicles Directorate 3550 Aberdeen Ave., SE Kirtland AFB, NM 87117-5776			**10. SPONSOR/MONITOR'S ACRONYM(S)** AFRL/RVSE
			11. SPONSOR/MONITOR'S REPORT NUMBER(S) AFRL-RV-PS-TR-2010-1039
12. DISTRIBUTION / AVAILABILITY STATEMENT Approved for public release; distribution is unlimited. (Clearance # RV10-0966, dtd 4 Jun 2010)			
13. SUPPLEMENTARY NOTES			
14. ABSTRACT The goal of this research was to develop an embedded magnetic memory technology to be integrated into a Complementary Metal Oxide Semiconductor (CMOS) fabrication process to provide radiation-hard, nonvolatile data storage. The benefits to spacecraft systems include the ability to power-down a subsystem while retaining system state, thus saving energy until the subsystem is required. This effort produced functioning magnetic tunneling junction MTJ) memory cells, but they did not achieve the desired resistance ratio. Two circuit designs were developed based on magnetic memory elements: a magnetic latch, and a magnetic shadow memory to serve as a backup to volatile electronic memory. Integrated Passive Electronic Components. The thrust of this effort is to develop new families of on-chip passive components, particularly inductors and programmable resistors. These supplement the transistors for which CMOS processing technologies are highly optimized. This work resulted in thin-film planar inductors that exhibit 50% greater inductance per unit area, and a 150% increase in Q, by using ferrite cladding contain and shape electromagnetic fields.			
15. SUBJECT TERMS SPACE VEHICLES; MAGNETIC RANDOM ACCESS MEMORY (MRAM); RECONFIGURABLE COMPUTING; MAGNETIC TUNNELING JUNCTION (MTJ) MEMORY CELLS			

16. SECURITY CLASSIFCATION OF:			**17. LIMITATION OF ABSTRACT**	**18. NUMBER OF PAGES**	**19a. NAME OF RESPONSIBLE PERSON** N. Shane Francis
a. REPORT UNCL	**b. ABSTRACT** UNCL	**c. THIS PAGE** UNCL	Unlimited	34	**19b. TELEPHONE NUMBER** *(include area code)*

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std. 239.18

(This page intentionally left blank)

Table of Contents

Section **Page**

List of Figures iv
Executive Summary v
1.0 INTRODUCTION 1
1.1 Magnetic Random Access Memory 1
1.1.1 MRAM Innovation 1
1.1.2 MRAM Benefits 1
1.1.3 MRAM Approach 2
1.2 Integrated Passive Components 2
1.2.1 Integrated Passives Innovation 2
1.2.2 Integrated Passives Benefits 2
1.2.3 Integrated Passives Approach 3
2.0 MTJ CELL DEVELOPMENT 4
2.1 Optimized PacMan “soft” magnetic element 4
2.2 Complete MTJ Cells 4
2.3 Storage Circuits Employing Magnetic Memory Cells 5
2.3.1 One-wire Writing Scheme 6
2.3.2 Single-wire Programming in Process Integration 6
2.3.3 Single-Wire Simulations 7
2.3.4 Integration into CMOS circuits 8
2.3.5 Results of Integration Study 11
3.0 INTEGRATED PASSIVES DEVELOPMENT 11
3.1 Ferrite-clad Inductors 11
3.2 Low-temperature Ferrites 15
3.3 Power Circuits and Digital Load 19
3.4 Programmable Resistors 20
4.0 CONCLUSION 21
BIBLIOGRAPHY 22
GLOSSARY 25

List of Figures

Figure **Page**

Figure 1: Ferrite-clad inductor 3
Figure 2: Final PacMan soft magnetic element 4
Figure 3: MTJ cell fabricated between orthogonal electrodes 4
Figure 4: Test array of MTJ cells 4
Figure 5: Differential magnetic flip flop. 5
Figure 6: Magnetic shadow RAM flip flop 5
Figure 7: Orientation of MTJ cells for opposite polarity. 6
Figure 8: One-wire writing configurations. 6
Figure 9: X-Y MTJ cell arrangement 7
Figure 10: Single-wire MTJ cell arrangement 7
Figure 11: Proposed MTJ cell structure for single-wire programming (not to scale) 8
Figure 12: Test structure for process integration 9
Figure 13: Process for fabricationg MTJ cells on short-loop structures 9
Figure 14: Text structures fabricated on American Semiconductor metal 10
Figure 15: Plot of surface roughness of FlexFET 6K metal 10
Figure 16: Three inductor cladding options 12
Figure 17: Inductance versus frequency for three inductor cladding options and air-core inductor 12
Figure 18: E-Field Distribution at 10 MHz. UA-SS is single-sided cladding (bottom only); UA-DS is double-sided cladding (top and bottom), and UA-C is enclosed cladding 13
Figure 19: H-Field distribution at 10 MHz. UA-SS is single-sided cladding (bottom only); UA-DS is double-sided cladding (top and bottom), and UA-C is enclosed cladding. 14
Figure 20: Comparison of air-core and ferrite inductors vs frequency 15
Figure 21: Schematic of particle beam acceleration 16
Figure 22: Graphic illustrating iron nanoparticle landing 16
Figure 23: Low-voltage, soft landing profile. 17
Figure 24: High-voltage, smooth film profile. 17
Figure 25: Magnetic field intensities for 0 kV film 18
Figure 26: Magnetic field intensities for 15-kV film 18
Figure 27: Iron nanoparticle with oxide coating. 19
Figure 28: Ion-conducting chalcogenide programmable resistor structure 20

Executive Summary

Magnetic Random Access Memory. The goal of this research was to develop an embedded magnetic memory technology to be integrated into a Complementary Metal Oxide Semiconductor (CMOS) integrated circuit fabrication process to provide radiation-hard, logic elements and small random-access memories. The goal is not to provide large-scale, bulk memory, but latches and flip flops that serve as state and data registers for sequential logic, and configuration registers for configurable logic. The benefits to spacecraft systems include the ability to power-down a subsystem while retaining system state, thus saving energy until the subsystem is required. The subsystem can then be powered-up and begin operating in milliseconds. The technology is based on a unique, PacMan-shaped magnetic tunneling junction (MTJ) cell developed at the University of Idaho. The focus of this research is to refine the PacMan cell to make it practical for integration into CMOS circuits, to develop CMOS circuits that employ the magnetic cells, and to integrate the cells onto a CMOS process. The produce produced two circuit designs based on magnetic memory elements: a magnetic latch, and a magnetic shadow memory to serve as a backup to volatile electronic memory.

Integrated Passive Electronic Components. The second thrust of this research is to develop new families of on-chip passive components, particularly inductors and programmable resistors. Today's CMOS processing technologies are highly optimized for making small, high-performance active components: transistors. Options for on-chip passive components, including resistors, capacitors, inductors and transformers, are limited. In particular, component values and quality (Q factor, or energy efficiency) of integrated passive components is very limited. Digital circuits are designed to work well without integrated passives, but analog circuits require quality passive components with a wide range of values. This includes the analog elements found on a digital chip, as well as devices designed for analog operation, including radio frequency (RF) and integrated mixed-signal devices such as analog-to-digital and digital-to-analog converters. Power supply circuits, such as DC-DC converters and voltage regulators also depend on quality passives. The ability to set passive component values electronically – to program them – would make possible a new kind of programmable analog circuits.

(This page intentionally left blank)

1.0 INTRODUCTION

This contract covers two technical areas: Magnetic Random Access Memory for Embedded Computing, and Integrated Passive Electronic Components. The original contract, FA9453-06-1-0355, from 1 Sep 06 to 11-30-07, covered third and last year of a three-year magnetic memory research effort. The contract was amended to add Integrated Passive Components. A no-cost extension was granted to extend the period of performance to 30 Nov 09.

The first task of this work was to develop an integrated magnetic memory technology, to provide low-power, nonvolatile, radiation-hard memory on a complementary metal oxide semiconductor (CMOS) process. This provides the means to create nonvolatile latches, flip flops, small amounts of random access memory, data registers, and nonvolatile lookup tables. The second task is to develop high quality passive components, particularly magnetic components (inductors), with a smaller effort aimed at programmable resistors. The inductor research is aimed at on-chip voltage conversion and regulation to provide reliable power for digital circuits on the same chip.

1.1 Magnetic Random Access Memory

1.1.1 MRAM Innovation

This research is based on these innovative elements: (1) the University of Idaho's unique magnetic element shape, which promises improved repeatability and reduced power consumption for memory writes; (2) Optimized thin-film fabrication process; (3) circuit designs to enable MRAM cells to be integrated into a CMOS process along with digital electronics, thus serving as distributed memory elements for latches and state and data registers.

1.1.2 MRAM Benefits

Radiation-hard, nonvolatile memory used in strategic parts of electronic systems offer increased responsiveness and reduced power consumption. A processor that uses nonvolatile memory for primary off-chip storage does not need to be "booted" after it is powered down; it can be powered back up in an "instant on" state, saving startup time and power. Nonvolatile Magnetic Tunneling Junction (MTJ) memory can provide this "instant on" capability. The magnetic storage cells themselves consume no power when not being accessed, and are inherently radiation hard. MTJ has the potential to serve as a key enabling technology for low-power processing and intelligent power management aboard power-critical systems, such as spacecraft. This will increase the quantity and quality of on-board data processing for a fixed power budget, enabling operational spacecraft to gather more and higher-quality data.

1.1.3 MRAM Approach

The major elements of the project are:

1. Develop and optimize a functional magnetic storage (MTJ) cell
    a. Develop an optimized "free" layer, whose magnetic orientation can be easily switched by a magnetic field.
    b. Develop a complete MTJ cell, incorporating the optimized free layer, whose resistance can be established by switching the magnetic polarity of the free layer.
2. Develop and model data storage circuits based on the MTJ cells.
3. Integrated the MTJ cells into a CMOS process.

The CMOS process chosen is the FlexFET™ Silicon-on-Insulator (SOI) developed by American Semiconductor, Inc., of Boise, ID, under the auspices of the Air Force Research Laboratory.

1.2 Integrated Passive Components

1.2.1 Integrated Passives Innovation

The primary innovations are (1) an improved design for planar inductors, using ferrite cladding to shape electromagnetic fields and minimize parasitic losses; (2) a method for low-temperature fabrication of ferrites with controlled electrical properties by means of accelerating beams of nanoparticles; (3) novel programmable resistors; (4) power circuits developed on the American Semiconductor FlexFET process to enable on-chip voltage regulation.

1.2.2 Integrated Passives Benefits

(1) The benefits of the novel inductor design are improved energy efficiency (quality factor or Q) and increased inductance values (L) for a given area. (2) The benefit of the low-temperature fabrication method is to enable high-quality inductors to be fabricated on the "back end" of a CMOS process without disrupting the characteristics of devices already fabricated on the die, particularly transistors. (3) The benefit of the programmable resistors is the ability to tailor or configure analog circuit behavior remotely, after the devices in fabricated, packaged and in the field. (4) The benefit of the power circuits is to enable power conditioning to be fabricated on the same die as the digital loads they power. This puts the power regulation on the "load side" of parasitic inductances that disrupt the power system, such as printed circuit board traces and package pins and bond wires. This will be an enabling technology for low-voltage, ultra-low-power electronics.

1.2.3 Integrated Passives Approach

The primary integrated passive component effort is to develop thin-film spiral inductors that are significantly more energy-efficient (higher Q) and capable of higher inductance per unit area than conventional methods by adding ferrite cladding. These inductors should be integrated onto digital chips at the back end of the CMOS fabrication process. This requires low-temperature processing, which is another effort under this contract. Finally, some novel, electrically-programmable resistors were developed.

The approach to efficient inductors is ferrite cladding. The ideal geometry for inductors is a helix, wound on a magnetic core. This is very difficult to achieve in integrated circuit processes, which are planar; the usual way to form inductors on CMOS chips is to deposit a planar spiral using aluminum normally used for interconnects. The resulting inductors are relatively easy to fit into the back-end fabrication process, but are limited in inductance value and in quality (Q), largely due to the inability to control the shape of the magnetic fields. The result is energy lost to the substrate (hysteresis losses), and opposing magnetic fringes, both of which decrease quality.

The solution is ferrite cladding, which shapes the electromagnetic fields to concentrate them where we want them, and to minimize losses to the substrate through fringing, and self-cancelling through opposing fields. The strategy is shown below for an inductor designed to operate at 10 MHz, a reasonable value for switching power converters. The ferrite cladding works optimally when applied to the top, bottom, and both sides of the coil.

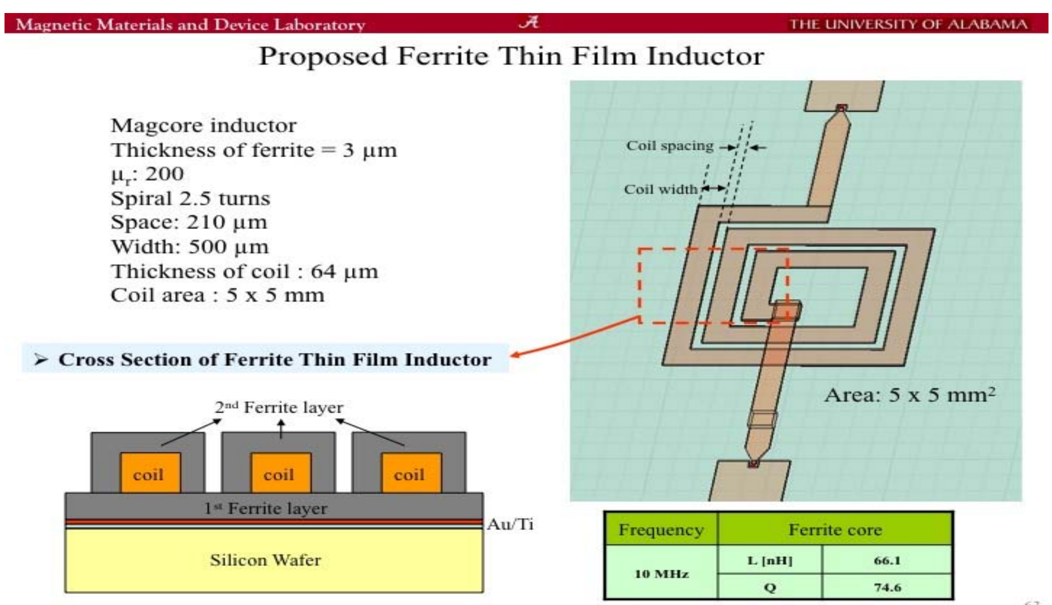


Figure 1: Ferrite-clad inductor.

2.0 MTJ CELL DEVELOPMENT

2.1 Optimized PacMan "soft" magnetic element

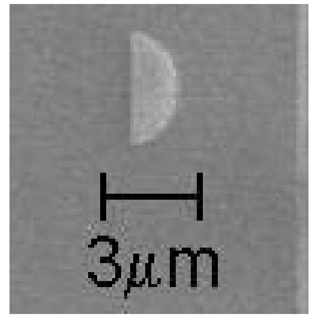


Figure 2: Final PacMan soft magnetic element.

The first challenge was to optimize the shape and material composition of the "free" magnetic layer to enable fast, reliable switching with a small amount of energy. The unique properties of the PacMan shape enable it to be programmed (i.e., forced into a particular magnetic polar orientation) repeatedly. Altering the details of the shape changes its switching properties, as does altering the material composition and size.

The team experimented with a variety of element compositions and shapes to achieve a set that had the desired properties. The primary parameter adjusted was the angle of the PacMan "mouth" opening. The optimal shape turned out to be defined by an arc on one side and a straight line on the other, as shown in Figure 2.

2.2 Complete MTJ Cells

Arrays of PacMan cells of different sizes and material compositions were designed and fabricated. Figures 3 and 4 show representative examples. The cells were fabricated between two orthogonal copper electrodes so their electrical properties could be read in a probe station. The cells were programmed with bulk magnetic fields (not electrically programmed) and their properties measured. The resulting cells had tunneling magnetic resistance ratios (TMR) ranging from 15% to 35%, and a nominal resistance of 10 to 15 Kilohms.

The cells had write currents ranging from 10 to 25 mA in short pulses, and switching times on the order of one to two nanoseconds. The write currents are higher than we would like, and we are working on ways to reduce them.

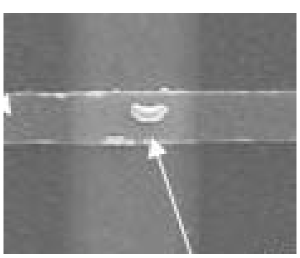


Figure 3: MTJ cell fabricated between orthogonal electrodes.

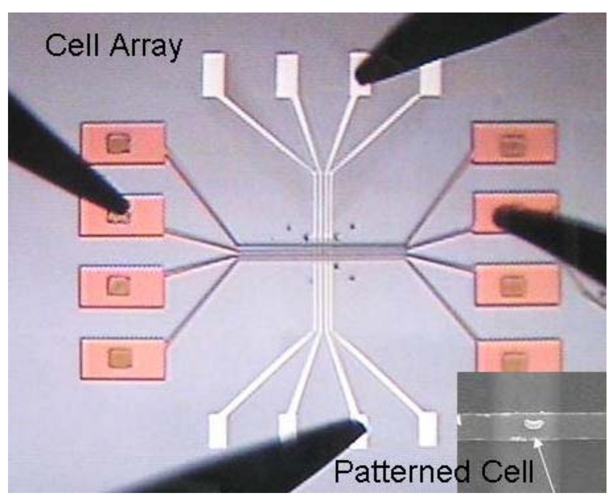


Figure 4: Test array of MTJ cells.

2.3 Storage Circuits Employing Magnetic Memory Cells

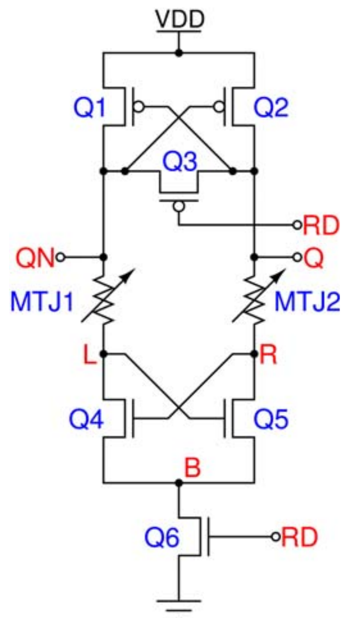


Figure 5: Differential magnetic flip flop.

Two kinds of circuits were designed and simulated.

- A differential magnetic flip flop
- A magnetic shadow flip flop

A circuit diagram of the differential magnetic flip flop is shown in Figure 5. MTJs are placed between the P and N halves of a 4-transistor latch The MTJs are programmed to opposite states In case of a single event upset, the flip flop will restore the original state as follows: One of the signals, L or R will fall faster than the other, due to the difference in MTJ resistance.

Positive feedback will force the appropriate output, Q or QN, to be low. The MTJs provide resistor isolation for SEU immunity

The magnetic flip flop takes advantage of the back gate of the FlexFET process. The circuit is shown in Figure 6. The MTJs are programmed to opposite states. During a restore operation, the back gates discharge at different rates, causing different voltages in Q1 and Q2. The MTJs operate in common mode.

This scheme is easily applied to a Single-Event Upset (SEU) immune cell such as the widely available DICE cell.

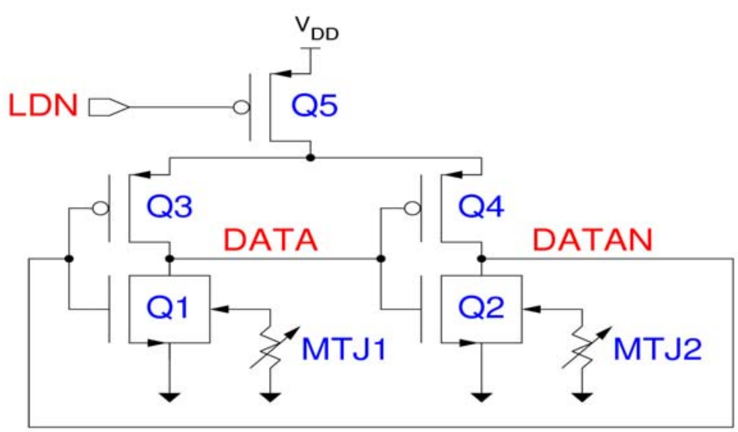


Figure 6: Magnetic shadow RAM flip flop.

2.3.1 One-wire Writing Scheme

Both of these circuits use one-wire writing. In this scheme, we abandon the X-Y addressing commonly employed in MRAMs. For the flip flop, we want the two MTJ cells to be programmed with opposite magnetic polarities. We achieve this by arranging the cells as shown in Figure 7. The write line is folded so the MTJ cells will experience magnetic fields of opposite senses from the same current.

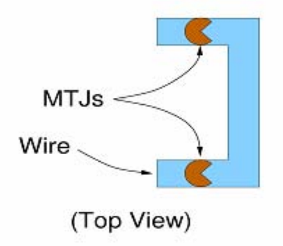


Figure 7: Orientation of MTJ cells for opposite polarity.

Figure 8(a) shows the magnetic fields (in green) from the electrical configuration shown, where current moves down the vertical metal run. In Figure 8(b), the writing current is reversed, and so are the magnetic fields generated by the currents. The switching scheme in Figure 8(c) can be implemented using drive transistors. In cases where banks of MTJ cells are to be written, as in data registers, the flip flops can be programmed in series, thus sharing a write current and minimizing the power required.

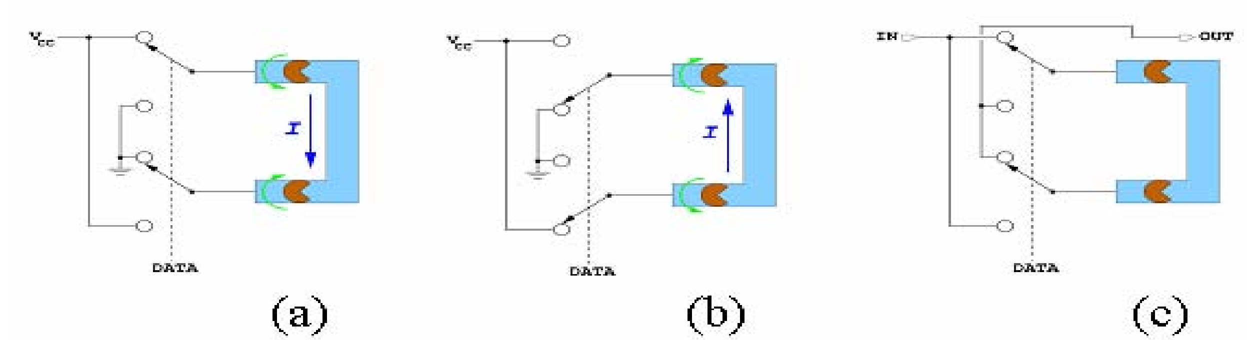


Figure 8: One-wire writing configurations.

The relatively small TMR of the MTJ cells and inevitable process variations suggested a differential circuit structure. We designed and simulated several versions, in the form of magnetic flop flops and shadow RAMs An interesting observation is that pairs of magnetic elements positioned in certain arrangements can share magnetic fields either constructively or destructively, which might be exploited to reduce write current [18].

2.3.2 Single-wire Programming in Process Integration

The usual MRAM architecture uses *two-wire programming*. It employs an X-Y array of MTJ cells, with a parallel set of metal conductors above the cells (e.g. bit lines) and an orthogonal set of conductors beneath (word lines), as shown in Figure 9. The MTJ cells are arranged with their magnetic axes at a forty-five-degree angle to both lines.   A cell is selectively written by driving its word and bit lines with a current that generates the electromagnetic fields whose vector sum causes the magnetic polarization of the selected cell to switch.

It is important that no other cell in the matrix is induced to switch – that is, the cells must be highly *selective*.

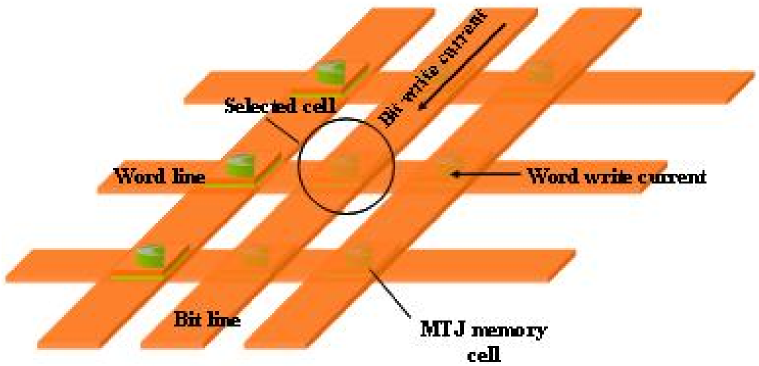


Figure 9: X-Y MTJ cell arrangement.

The two-wire programming scheme presents a challenge for back-end CMOS processing. It is desirable to use existing metal layers to program the cells. However, at reasonable currents, on the order of 20 mA, the required distance between the conductors and the cells is small, on the order of ten microns. The MTJ cell is about 40 nm tall. The space between metal layers in the 0.25 micron CMOS process is about 100 microns. The cells cannot be placed between metal layers such that they are close enough to both metal lines to generate a strong enough electromagnetic field at reasonable currents.

Two possible solutions are to develop a back-end metal process that meets the space requirements, or to abandon the X-Y two-wire scheme, and use single-wire programming. This project pursued the latter option.

2.3.3 Single-Wire Simulations

Figure 10 shows the arrangement for single-wire programming. For optimal programming, the MTJ cell must be placed at the proper angle with respect to the magnetic field, and hence to the programming, which is orthogonal to the field. The optimal angle is generally accepted to be about 45 degrees. To investigate ideal placement and assess feasibility, we modeled an MTJ cell at different angles with respect to the current.

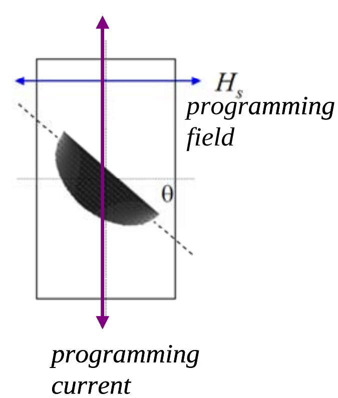


Figure 10: Single-wire MTJ cell arrangement.

The Pac Man I (PM I) shape was chosen, in which the notch is opened to 180 degrees, or a straight line. The experimental parameters are:

Proposed Scenario

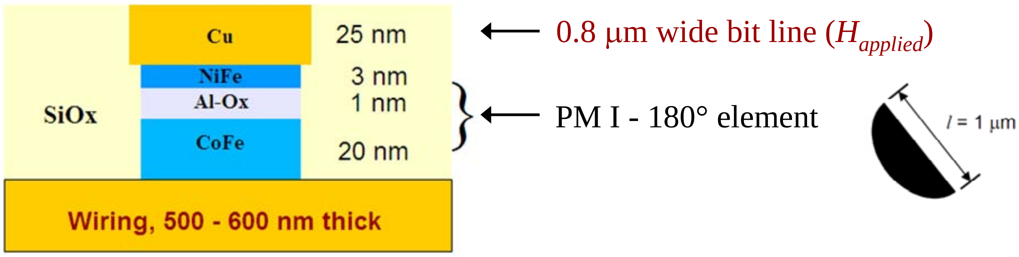


Figure 11: Proposed MTJ cell structure for single-wire programming (not to scale).

A workable scenario is to $1\,\mu m \times 0.36\mu m$ Pac Man I 180-degree cell with the cross-section shown, at 30 degrees orientation, sandwiched between an aluminum conductor and a copper write line. With this arrangement, a current pulse of 11.8 mA, lasting about 2.5 ns, creates a magnetic field strength of 90 Oersteds, sufficient to completely switch the cell. For logic purposes, the switching is virtually complete after 1.2 ns.

2.3.4 Integration into CMOS circuits

American Semiconductor, Inc., of Boise was selected as a CMOS integrated circuit partner. Their radiation-hard FlexFET™ Silicon-on-Insulator CMOS process was developed under the guidance of AFRL/RVSE for aerospace applications. Unlike large IC production companies, American Semi specializes in custom, developmental work of this sort, and proved to be very willing to work with us.

The FlexFET™ process has the following advantages:

- High-performance “Silicon on Insulator” technology
- Ability to adjust operating voltage, which is exploited in another University of Idaho program for ultra-low-power microelectronics. This is the technology that can benefit most from our integrated passive components.
- Radiation hard for space applications.
- Fabricated at an on-shore U.S. facility (Cypresss Semiconductor in California)

The first step was to determine whether MTJ cells can actually be fabricated on on American Semiconductor’s metal.

To determine this, a test array was designed and fabricated in a “short loop” cycle on the American Semiconductor process. The short loop cycle produces test wafers, but does not go through the entire integrated circuit fabrication process. In this case, the short loop tests only go through the field oxide and metal deposition steps. Figure 12 below shows the test structure. It consists of horizontal and vertical traces. The horizontal traces represent the lower

metal level, and the vertical traces the upper level. The vertical traces are not complete: they leave a gap where the MTJ cell array is to be fabricated.
After the metal structures are fabricated, the wafers are removed from the fabrication line and diced. In the lab, the MTJ cells are deposited, and the upper metal traces completed.

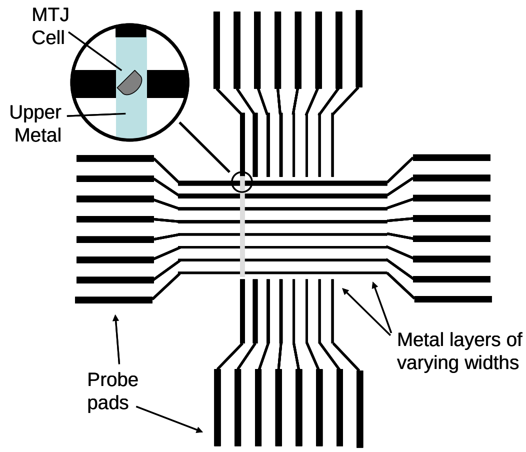


Figure 12: Test structure for process integration.

Figure 13 shows the process used to fabricate the test cells onto the FlexFET metal. Figure 14 is a photograph of the metal test structures. Figure 15 is an Atomic Force Microscope image of the MTJ cells fabricated on the metal test structures. The grain boundaries of the underlying aluminum are clearly visible.

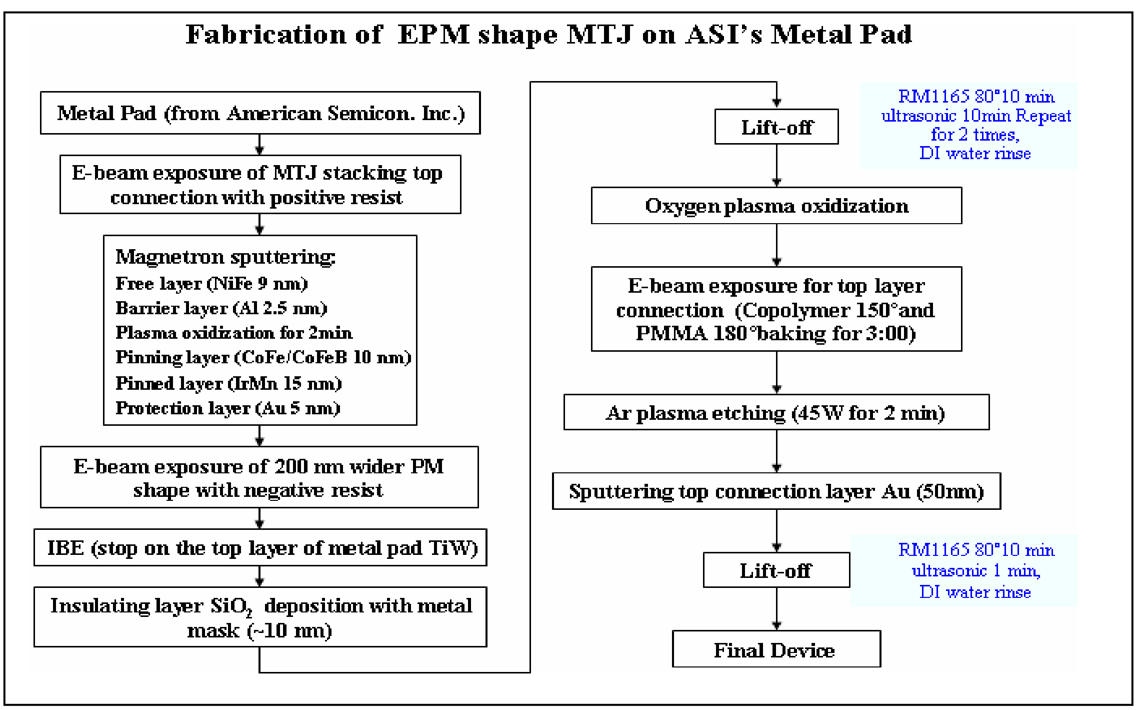


Figure 13: Process for fabricating MTJ cells on short-loop structures.

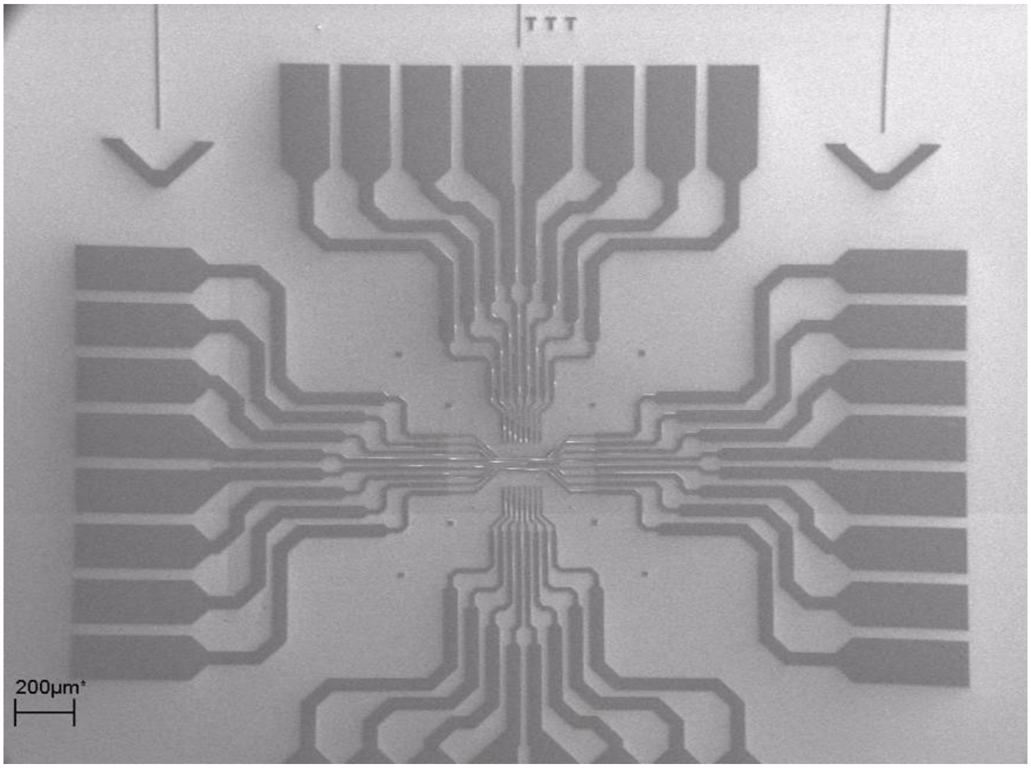


Figure 14: Test structures fabricated on American Semiconductor metal.

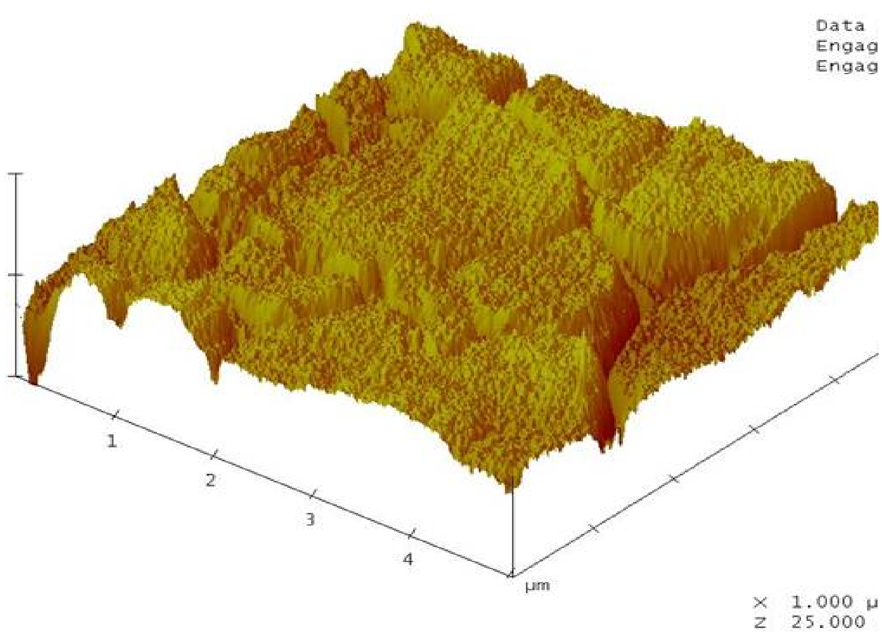


Figure 15: Plot of surface roughness of FlexFET 6K metal.

2.3.5 Results of Integration Study

MTJ cells were successfully fabricated on the FlexFET metal, but the performance of these cells was disappointing. The first issue to address is the surface roughness of the FlexFET metal, which seems to affect MTJ cell performance. The MTJ cells are only about 40 nm high, comparable to the roughness of the metal. The MTJ cells tend to follow the contour of the metal, and the resulting shape destroys their desired electrical properties.

The team considered the following choices to mitigate the roughness problem:

1. Select a different metal layer. The top metal (20K) is smoother than the others, so we should work with it first.
2. Polish the surface with Chemical-Mechanical Polishing (CMP)
3. "Decorate" the grain boundaries and etch back. For example, we have used spin-on glass (SOG), followed by ion beam etching.
4. Optimization of the Al deposition temperature.
5. Select a different material on which to fabricate MTJ cells.

Option 2 has showed little success. Option 3 has reduced the RMS roughness from 4.65 to 3.16 nm, and cut the peak in half from 28.88 to 15.23 nm. Option 4 and 5 require a new fabrication runs. The team decided to pursue option 5, fabricating MTJ cells onto a tungsten surface, which is much smoother than aluminum. This was carried out under a separate contract, and the results will be reported accordingly. The results were encouraging.

3.0 INTEGRATED PASSIVES DEVELOPMENT

The integrated passives element consists of (1) area- and power-efficient, ferrite-clad spiral inductors; (2) low-temperature ferrite processing; (3) power and digital load circuits; (4) programmable resistors.

3.1 Ferrite-clad Inductors

Real inductors (and capacitors) must be designed to operate in a particular frequency range, as parasitic characteristics cause different behaviors at different frequencies. For this study, we assumed the inductors would be used for on-chip power conversion and regulation using a switching topology, switching at 5 MHz. The specifications chosen for the inductor were:

- 5 MHz operating frequency
- 125 nanohenry inductance
- Q > 50
- Input voltage: 5V
- Output voltage: 1, 0.5 and 0.25 V at 1 watt
- Current capacity: Up to 1A
- Substrate: Si wafer

Three different configurations were explored initially:

1. Ferrite cladding on bottom surface only
2. Ferrite on top and bottom
3. Ferrite on top, bottom and sides

Not surprisingly, the more complete the ferrite cladding, the higher the achievable inductance, as shown in the plots in Figures 16 and 17.

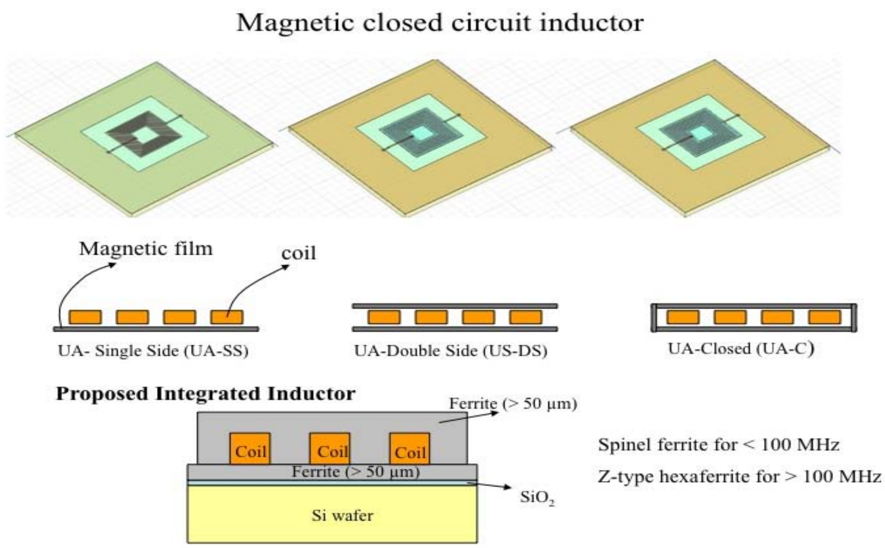


Figure 16: Three inductor cladding options.

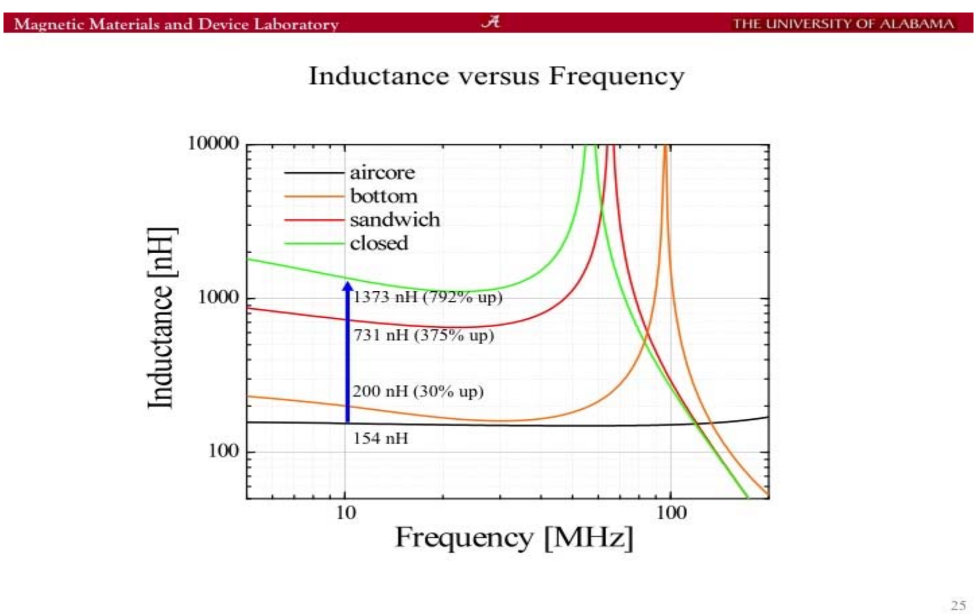


Figure 17: Inductance versus frequency for three inductor cladding options and air-core inductor.

The effects of the ferrite cladding are evident when we look at the electric E-field and H-field distributions, as shown in Figures 18 and 19 below. The idea is to use ferrite cladding to contain the electromagnetic fields where we want them within the coils. This minimizes destructive interference between coils, increasing L, and minimizes losses from field fringes transferring energy to the substrate, thus increasing Q.

In these two figures, the fringe field strengths are enhanced by the ferrite cladding. Fringe fields are evident in the single sided cladding, reduced in double-sided cladding, and significantly reduced in the enclosed cladding.

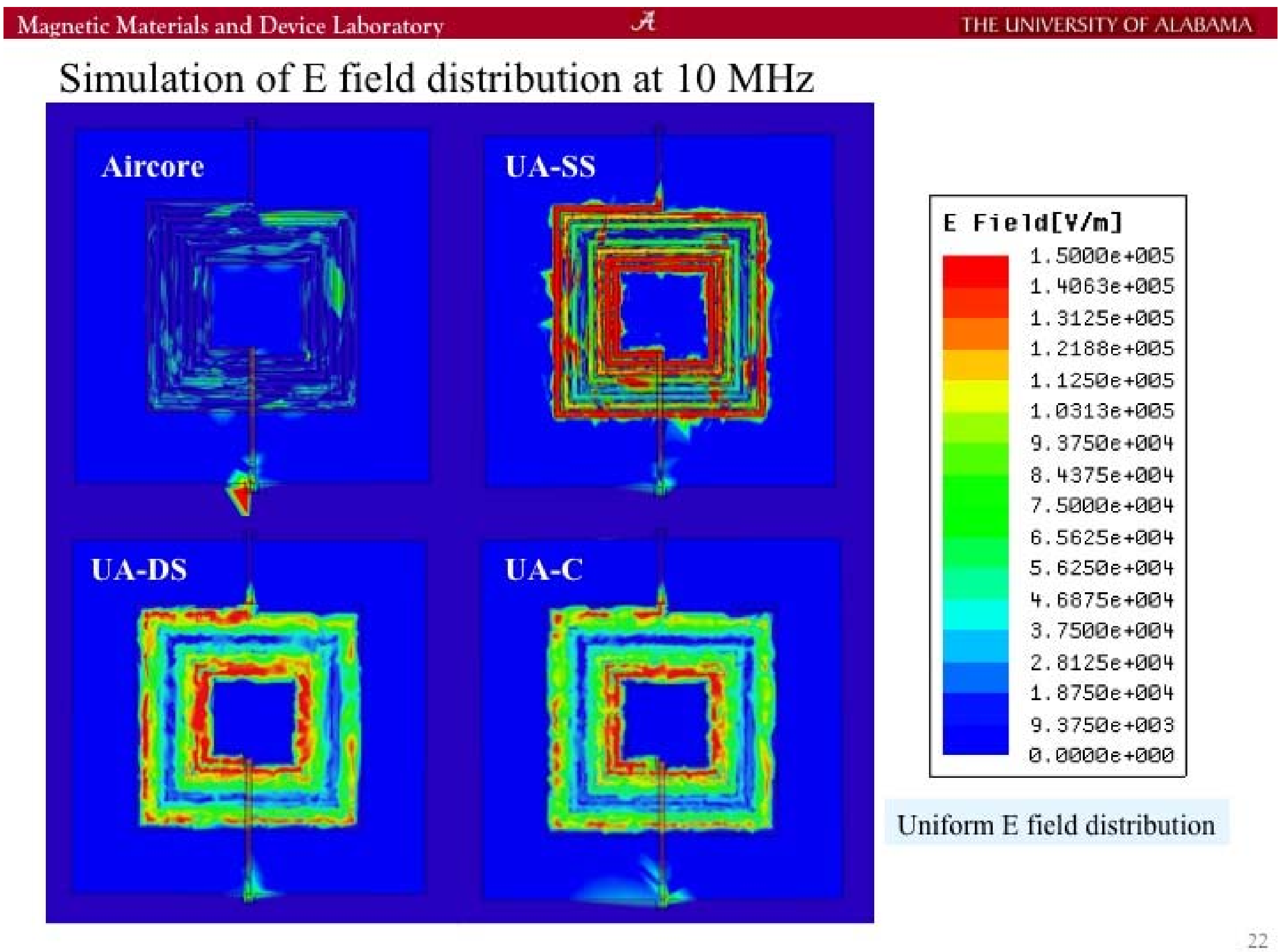


Figure 18: E-Field Distribution at 10 MHz. UA-SS is single-sided cladding (bottom only); UA-DS is double-sided cladding (top and bottom), and UA-C is enclosed cladding.

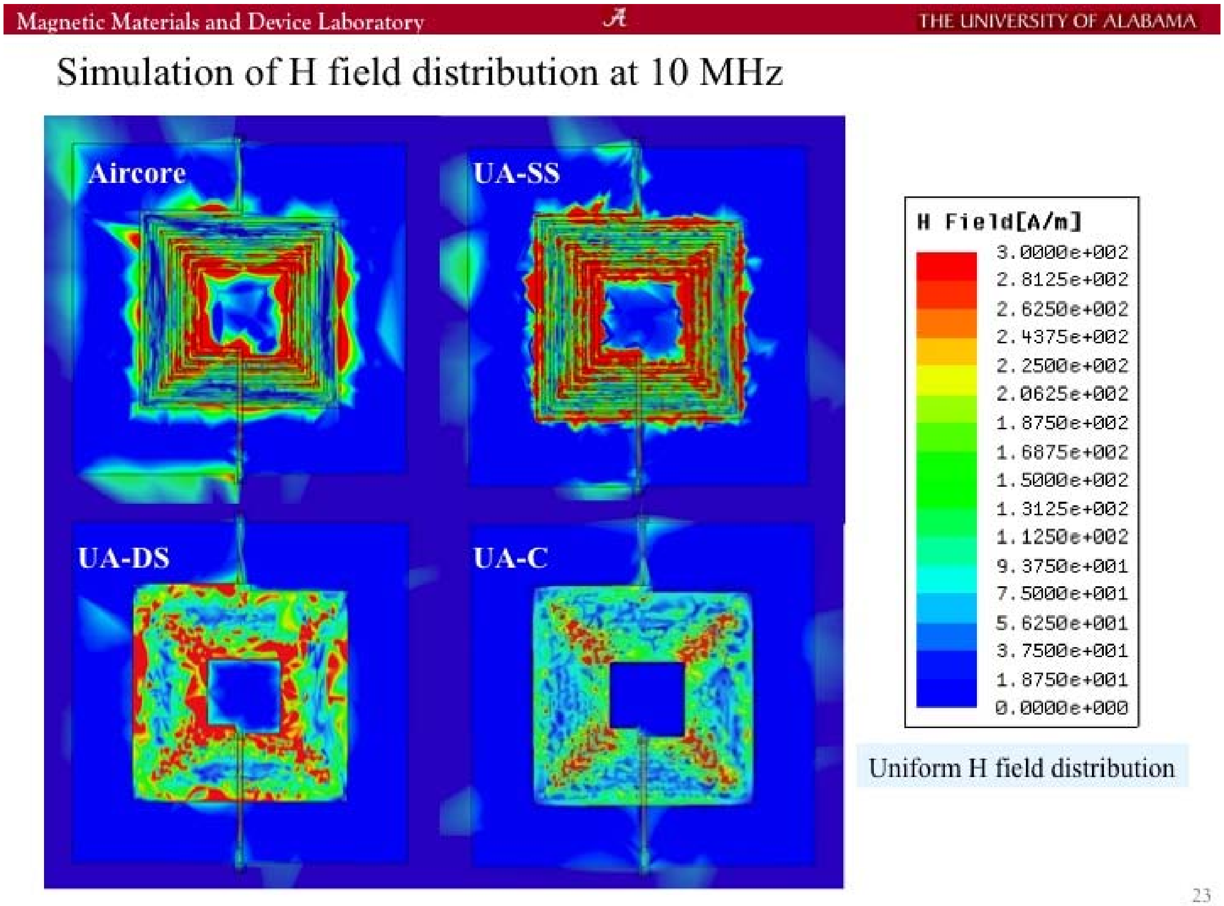
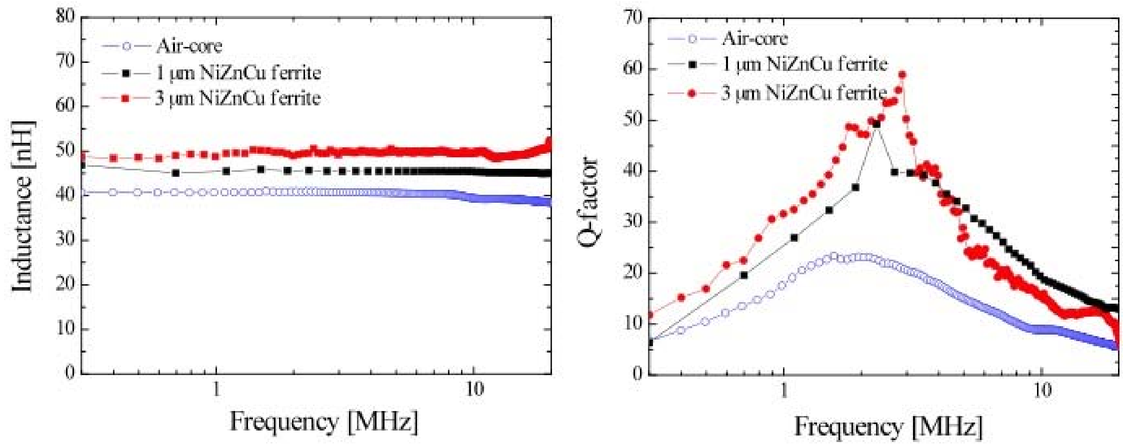


Figure 19: H-Field distribution at 10 MHz. UA-SS is single-sided cladding (bottom only); UA-DS is double-sided cladding (top and bottom), and UA-C is enclosed cladding.

Inductors were designed and optimized for 5 MHz using Computer-Aided Design (CAD) software. Air-core and ferrite inductors were fabricated and measured. Details are in the appendix. Relative performance is shown in Figure 20 below. Three-micron ferrite increased the Q by over 150%.

Magnetic Materials and Device Laboratory THE UNIVERSITY OF ALABAMA

Inductances and Q-factors of Air-core and Ferrite Inductors



4.5 turns	Air-core	1 μm ferrite	3 μm ferrite
Inductance [nH]	40.8	45.5	50.0
Max. Q-factor	23.2	49.3	59.0

➤ Ferrite inductor shows 22.5 % increase in inductance and 113 and 154 % increase in Q-factor with 1 and 3 μm ferrite, respectively.

92

Figure 20: Comparison of air-core and ferrite inductors vs frequency.

3.2 Low-temperature Ferrites

The plan for this project is to fabricate ferrite-clad inductors at the back-end-of-line (BEOL) CMOS process, after the active components have been created. Back-end processing is subject to temperature constraints, as temperatures greater than about 600C cause metals to melt and implants and diffusions to migrate. Ferrites are typically fabricated at 900 C, making them unsuitable for BEOL processing. Therefore, and alternative, low-temperature ferrite process was sought.

The solution was accelerate iron nanoparticles to a target, where they built up like snowballs thrown against a wall. The particles are accelerated through an electric field ranging from 0 to 40 kV. The accelerating voltage affects the roughness of the film, as well as the magnetization properties. Figure 21 is a schematic of the process. Figure 22 depicts the landing of the iron nanoparticles on the target. Figures 23 and 24 show the low-voltage and high-voltage film roughness characteristics, respectively. Figures 25 and 26 show the angular magnetic profile for the two cases.

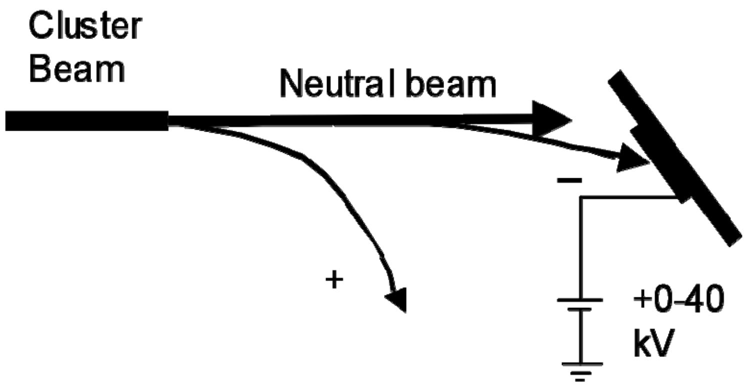


Figure 21: Schematic of particle beam acceleration.

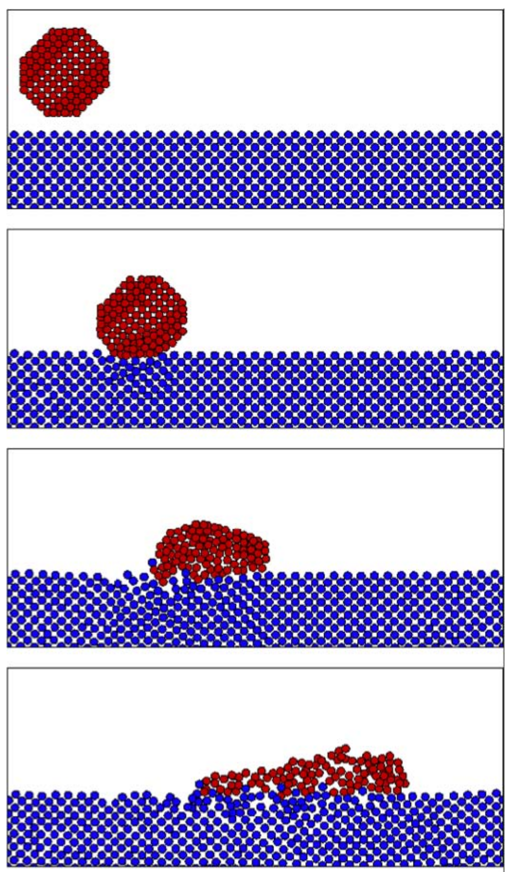


Figure 22: Graphic illustrating iron nanoparticle landing.

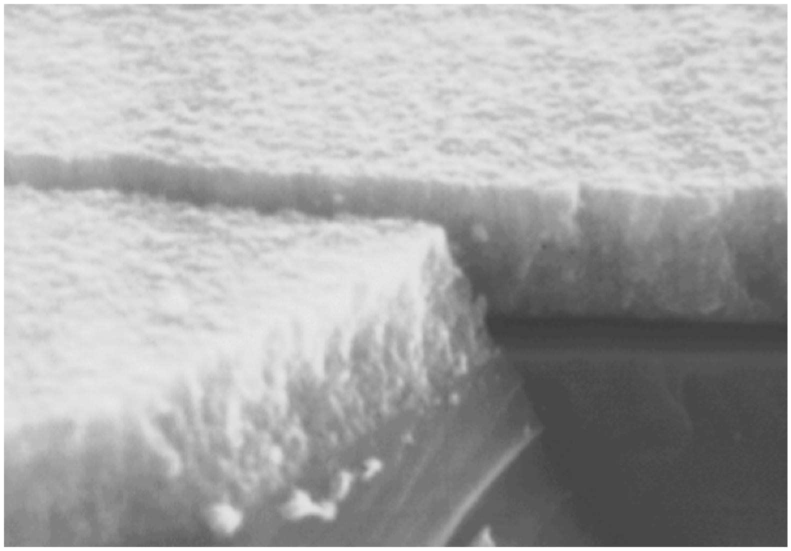


Figure 23: Low-voltage, soft landing profile.

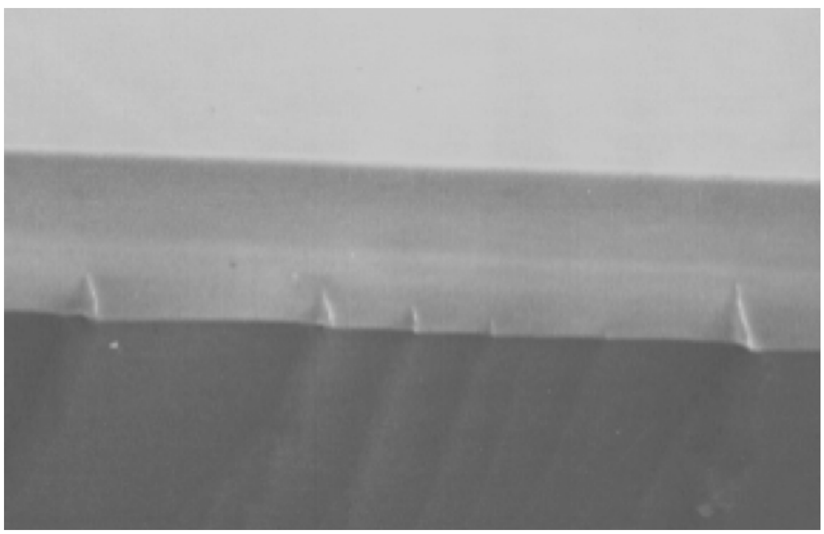


Figure 24: High-voltage, smooth film profile.

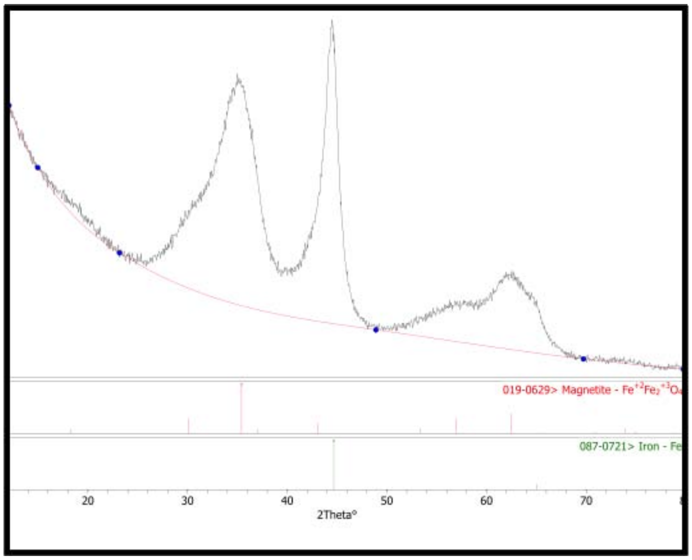


Figure 25: Magnetic field intensities for 0 kV film.

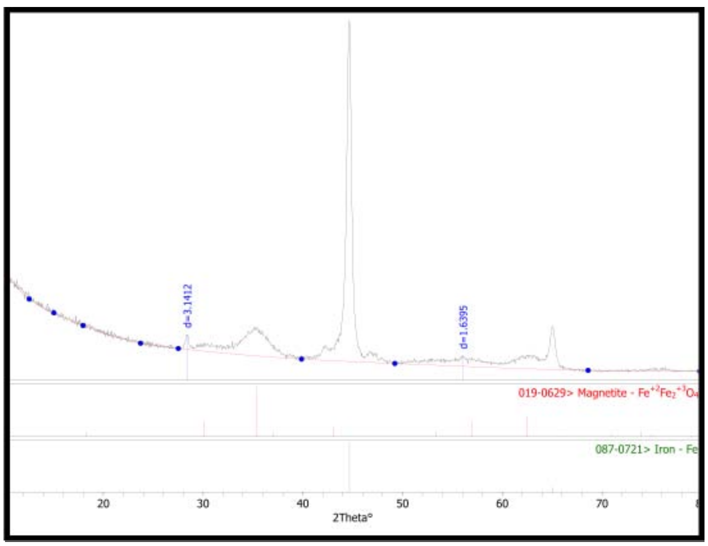


Figure 26: Magnetic field intensities for 15-kV film.

In addition to film roughness and magnetic moments, we can control the resistivity of the particles by accelerating them through an oxygen gas. This causes an oxide shell to form. By controlling the density of the gas and the acceleration velocity, we can control the thickness of the shell, and hence the resistivity of the film. Figure 27 shows a particle with an iron core and oxide shell.

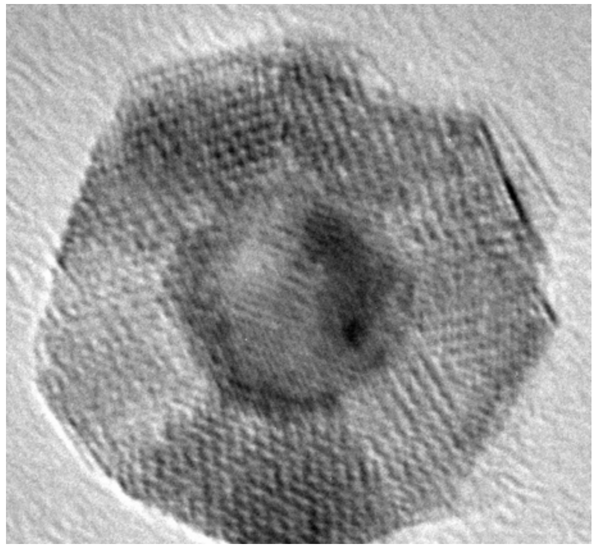


Figure 27: Iron nanoparticle with oxide coating.

3.3 Power Circuits and Digital Load

The target CMOS process for this work is the American Semiconductor FlexFETTM, a silicon-on-insulator process developed under AFRL auspices for space applications. Available at 0.25 and 0.18 micron process nodes, the process is unique in that it is provided with a “back gate”, making it possible to adjust the substrate bias voltage, and therefore the switching threshold. This makes the process ideal for ultra-low-power operation by reducing the supply voltage to ½ to ¼ volt. Dynamic power consumption decreases as the square of the supply voltage, but leakage increases as the switching threshold is reduced. The ideal operating point for power savings is where dynamic and static power consumption are about equal.

Low-voltage operation has the potential to save power, but it also creates the problem this research addresses: delivery of stable, well-regulated power to the gates on the chip. The conventional approach to providing DC power is to place voltage regulators on a circuit board and route the power and ground connections to the package pins of the chips. The operating chip draws bursts of current from the power supply, causing inductive voltage drops in PCB traces, package pins and bond wires. Careful PCB power routing and coupling capacitors placed at the pins of the chips help compensate for inductive losses, but at very low voltage, this may not be adequate to provide stable power at the gates.

An alternative is point-of-load voltage regulation on the chip itself, on the load side of PCB traces, package pins and bond wires. High-quality passive components are critical to successful voltage regulation, but so are on-chip power circuits. The FlexFET™ process is optimized for digital and radio frequency circuits – a development effort was required to determine whether, and how, to use the process features to implement power circuits.

Four different test circuits were designed and fabricated. One is a digital load – in this case, a design already at hand, a processing element from the Field Programmable Processor Array (FPPA).

The other three were power circuits, designed to these parameters:

- 2.5V source voltage to the chip (compatible with ASI process)
- V_{DD} = 1V for digital load
- 1 Watt average digital load (1 Amp)
- Switching frequency = 5-10 MHz

The evaluation criteria are:

1. Circuit area and complexity
2. Conversion efficiency
3. Ability to handle required current and voltages
4. Ripple control
5. Regulation stability

The test circuits are:

1. Digital load. To prove the concept of on-chip point-of-load power, a digital load circuit was created. This is a design already at hand: a processing element from the Field Programmable Processor Array.
2. A buck converter with a transistor array.
3. A full bridge converter with a diode array.
4. A resonant converter

The full bridge converter has been completely tested. It was not fully functional. This was traced to discrepancies in the process models. The process models were updated as a result of this. New samples are planned for fabrication in follow-on work.

3.4 Programmable Resistors

Programmable resistors were developed and demonstrated under subcontract to Boise State University. The structure is shown below. Based on ion-conducting chalcogenide devices, devices were fabricated and demonstrated in bench-top applications. The devices were packaged in 16-pin packages, 8 devices to a package. Example circuits are a rectifier, an electro-static protection device, and a phased-locked loop.

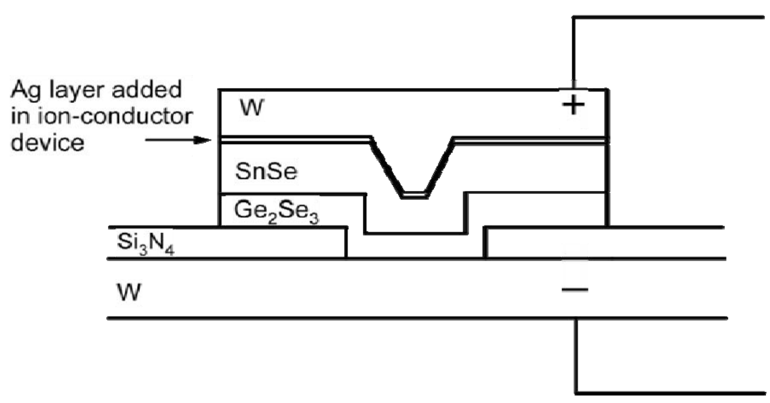


Figure 28: Ion-conducting chalcogenide programmable resistor structure.

4.0 CONCLUSION

The project produced workable magnetic tunneling junction (MTJ) memory cells, which were programmed in a bulk magnetic field. In the process, the researchers learned and published many details about the switching behavior of magnetic devices, which have an impact on the optimal design of these devices. A feasible set of latch and shadow RAM circuits was developed and modeled.

The specifications for the MTJ cells required for successful implementation of the magnetic latches are:

- Nominal resistance: 10 KΩ
- Tunneling Magnetic Resistance Ratio (TMR): 15%
- The preferred size and shape is an elongated PacMan, 1 µm in length

Integrating the MTJ cells onto a CMOS process proved elusive because of the difficulties in creating a metal surface smooth enough to accept the cells. This is necessary in order to carry out the next phases of the research, i.e., to develop accurate electronic circuit (SPICE) models, to implement the on-wire writing scheme, and finally, to integrate MTJ cells with CMOS electronics. This work is being carried out in a follow-on project.

Since patterned test cells were not available, due to the roughness problem described above, it has not been possible to test the one-wire writing concept. Simulations indicate that the write current pulses will have to be 20 mA for about 3 ns. This is much higher than desired. Some approaches will be studied to enable writing the cells with much lower current. The most promising is to clad the cells with a magnetic material that focuses the magnetic field onto the cell, where it is needed.
Ferrite-clad thin film inductors were successfully conceived, modeled, designed, and tested. The results were very positive: compared to air-core inductors, the ferrite-clad inductors exhibit a significantly higher quality factor.

Power and digital circuits were designed and fabricated. Some failed to function because of discrepancies in process models; the process models have consequently been updated.

Programmable resistors were developed, fabricated, and tested in several demonstration applications.

BIBLIOGRAPHY

S. Bae, Y.-K. Hong, J.-J. Lee, J. Jalli, G.S. Abo, A. Lyle, B.C. Choi, and G.W. Donohoe, “High Q Ni-Zn-Cu Ferrite Inductor for On-Chip Power Module”, IEEE Trans. Magnetics, Vol. 45, No. 10, October 2009.

S. Bae, Y.-K. Hong, J.-J. Lee, L. Jalli, G. Abo, B.C. Kim and G.W. Donohoe, “High Q ferrite film inductor for on-chip power module”, IEEE International Magnetics Conference, Sacramento, CA, May, 2009.

S. Bae, Y.-K. Hong, J.-J. Lee, G. Abo, J. Jalli,A. Lyle, H. Han, and G. W. Donohoe, “Optimized Design of Low Voltage High Current Ferrite Planar Inductor for 10 MHz On-chip Power Module”, Journal of Magnetics 13(2), 37-42 (2008).

S. Bae, Y. K. Hong, J. J. Lee, G. S. Abo, J. Jalli, A. Lyle, and G. W. Donohoe, “High Q Ni-Zn-Cu ferrite inductor on-chip power module,” Digest No. AG-04, 2008 IEEE International Magnetics Conference, Madrid, Spain, May 4 - 8, 2008.

S. Bae, Y.K. Hong, J.J. Lee, G.S. Abo, J. Jalli, A. Lyle, H. Han, and G.W. Donohoe, ” Optimization of Design Parameters for Ferrite Inductor for 10 MHz On-chip Power Module”, 2008 IEEE International Magnetics Conference, Madrid, Spain, May 4 - 8, 2008.

S. Bae, Y. K. Hong, J. J. Lee, J. Jalli, G. S. Abo, A. Lyle, H. Han, G. W. Donohoe, “Optimization of design parameters for ferrite inductor for 10 MHz on-chip power module,” Digest No. CQ-12, accepted for presentation at the 2008 IEEE International Magnetics Conference, Madrid, Spain, May 4 - 8, 2008.

B. C. Choi, J. Rudge, Y.-K. Hong, A. Santoni, J. Kolthammer, S. Gavin and G.W. Donohoe, “Surface roughness induced magnetic damping in $Ni_{80}Fe_{20}$ thin films investigated by in-situ time-resolved Kerr microscopy”, Proc. 11th Joint MMM-Intermag Conference, Washington, DC, January 2010.

B. C. Choi, Y. K. Hong, J. Rudge, J. E. Girgis, J. Kolthammer, A. Lyle, and G. W. Donohoe, “Switching of vortex chirality in $Ni_{80}Fe_{20}$/Cu/Co nanopillars by a spin-polarized current pulse” Digest No. HD-04, 2008 IEEE International Magnetics Conference, Madrid, Spain, May 4 - 8, 2008.

B. C. Choi, Y. K. Hong, J. Rudge, E. Girgis, J. Kolthammer, and G. W. Donohoe, “Nonequilbrium process of magnetization switching influenced by thermal spin fluctuation (Invited),” Phys. Stat. Sol., Dec 2007.

J. Founds, *A Partially Integrated Full-Bridge DC-DC Converter with Phase-Locking Control*, Master of Science Thesis, Electrical Engineering, December, 2009.

K.J. Hass, G.W. Donohoe and Y.K Hong, “Integrated Magnetic Memory for Embedded Computing Systems, IEEE Aerospace Conference, Big Sky, MT, March 3-10, 2007.

K.J. Hass, *Radiation-Tolerant Embedded Memory using Magnetic Tunnel Junctions*, Ph.D. Dissertation, Electrical Engineering, University of Idaho, May, 2007.

J-J Lee, Y.-K. Hong, S. Bae, Ji-H. Park, J. Jalli, S. Gavin, B.-C. Choi, and G.W. Donohoe, “High quality factor Ni-Zn Ferrite Planar Inductor”, to appear, Proc. 11th Joint MMM-Intermag Conference, Washington, DC, January 2010.

J-J. Li, Y.-K. Hong, S. Bae, J B. C. Choi, Q. F. Xiao, Y. K. Hong, J. Rudge, and G. W. Donohoe, “Vortex core switching dynamics in submicron permalloy disk,” IEEE Transactions on Magnetics, Vol. 43, No. 6, pp. 2926-2928 (2007).

A. Lyle, Y.-K. Hong, B.-C. Choi, G.S. Abo, M.-H. Park, S.-H. Gee, J. Jalli, S. Bae and G.W Donohoe, “Spin-Polareized current Switching of Co/Cu/Py Elongated Pac-Man Spin-Valve”, IEEE Trans. Magnetics, Vol. 45, No. 6, June, 2009.

A. Lyle, Y.-K. Hong, B.-C. Choi, G. Abo, J. Jeevan, R. Syslo, S. Bae, J.-J. Lee, M.-H. Park, and G. W. Donohoe, “Magnetic field switching of 8x8 array of Co/Cu/Py elongated and type II Pac-man spin valves,” Proc. IEEE International Magnetics Conference, Sacramento, CA, May, 2009.

A. Lyle, Y.-K. Hong, B.-C. Choi, G. Abo, J. Jeevan, R. Syslo, M.-H. Park and G.W. Donohoe, “Spin-polarized current switching of Co/Cu/Py Pac-man type II”, Proc. IEEE International Magnetics Conference, Sacramento, CA, May, 2009.

A. Lyle, Yang-Ki Hong, Byoung-Chul Choi, Gavin Abo, Hongmei Han, Jeevan Jalli, Soek Bae, Jae-Jin Lee, Patrick LeClaire, Ran Syslo, Gregory Donohoe and Sung-Hoon Gee, “Spin-polarized current stimulation of 100 nm dual vortex Co/Cu/Py spin valve nanopillars”, to appear, Proc. Magnetism and Magnetic Materials Conference, Austin, TX, Nov. 2008.

ZA. Lyle, Y. K. Hong, B. C. Choi, J. Rudge, G. S. Abo, S. H. Gee, H. M. Han, J. Jalli, and G. W. Donohoe, “Fabrication of 8x8 array of spin valve pillars and MR characterization,” Digest No. AS-01, Proc. IEEE International Magnetics Conference, Madrid, Spain, May 4 - 8, 2008.

D. Meyer, M. Faheem, M. Campanell, J. Antony, A. Sharma and Y. Qiang, “Magnetic Nanocrystalline Films Softened by Obliquely Accelerating Iron Nanoclusters”, IEEE Transactions on Magnetics, VOL. 43, NO. 6, June 2007.

J.-H. Park, J. Jalli, G. Abo, r. Syslo, B. Choi, G. W. Donohoe, “High quality Ni-Zn ferrite planar inductor,” to appear, IEEE Trans. Magnetics, November 2009.

Y. Quiang, D. Meyer, Y. Tian, R. Souza and G. Donohoe, “Soft magnetic composites generated by energetic iron/iron oxide core-shell nanocluster impact, Magnetism and Magnetic Materials Conference, Austin, TX, Nov. 2008.

Q. F. Xiao, B.C. Choi, J. Rudge, Y.K. Hong and G.W. Donohoe, “Vortex core dynamics in submicron ferromagnetic disks”, Joint Magnetism and Materials/Intermag Conference (AIP/IEEE), Baltimore, MD, Jan 7-12, 2007.

Q.F. Xiao, B.C. Choi, J. Rudge, E. Giris, J. Kolthammer, Y.K. Hong and G.W. Donohoe, “Dynamics of magnetic vortex core switching in Fe nanodisks by applying in-plane magnetic field pulse”, Journal of Applied Physics 102, 103904 (2007).

Q. F. Xiao, B. C. Choi, Y. K. Hong, J. Rudge, and G. W. Donohoe, “Effect of magnetic field pulse on ultrafast magnetization reversal in submicron elliptical permalloy thin film,” Journal of Applied Physics, Vol. 101, no. 1, 024306 (2007).

GLOSSARY

BEOL – Back End of Line Processing. The later steps in integrated circuit fabrication, where metal interconnects are deposited.

CAD – Computer-Aided Design

CMOS – Complementary Metal-Oxide Semiconductor.

CMP – Chemical-mechanical polishing. A polishing method that includes a corrosive material along with abrasives.

DC – Direct (as opposed to alternating) current.

DC-DC Converter. A circuit to convert one DC level to another, usually to supply power at a specified DC voltage. Also implies voltage regulation.

DICE Cell – Dual Interlocked Storage Cell. A memory cell designed with built-in redundancy to mitigate Single Event Upset (SEU) radiation effects.

FlexFET™ – a proprietary SOI CMOS process developed by American Semiconductor, Inc., Boise, ID, for aerospace applications.

MRAM – Magnetic Random-Access Memory.

MTJ – Magnetic Tunneling Junction, a form of magnetic memory structure.

Q – Inductor quality factor. Ratio of inductive reactance to resistance.

Pac-Man shape - An experimental shape for magnetic tunneling junction memory cells, so called because it resembles the character in the popular video game of that name.

PCB – Printed Circuit Board.

RF – Radio Frequncy.

RMS – Root-mean-square. RMS roughness is a characterization of the texture of a surface, a measure of average deviation from the perfectly smooth.

SEE – Single Event Effects. Changes in state or behavior a electronic circuits caused by being struck by an energetic ion, a component of cosmic radiation. SEE include Single Event Upset, Single Event Latchup, and Single Event Transients.

SEL – Single Event Latchup. Pathological state in CMOS circuits caused by an ion strike.

DISTRIBUTION LIST

DTIC/OCP 8725 John J. Kingman Rd, Suite 0944 Ft Belvoir, VA 22060-6218	1 cy
AFRL/RVIL Kirtland AFB, NM 87117-5776	2 cys
Official Record Copy AFRL/RVSE/N. Shane Francis	1 cy